Application Report

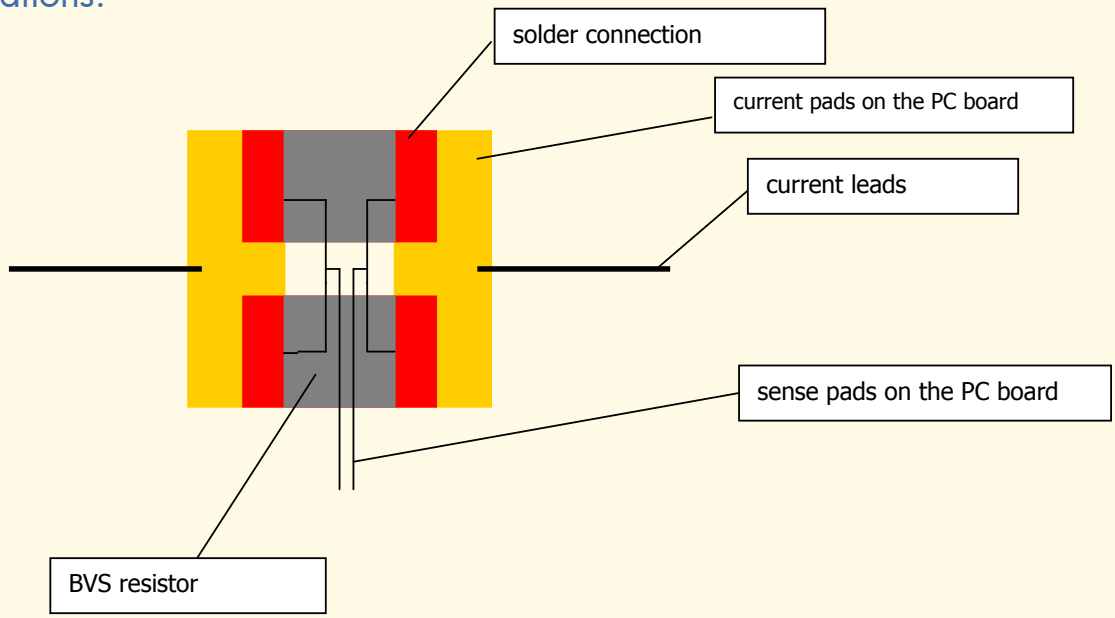
Parallel connection of BVS resistors

It is known that for parallel connected low-ohmic resistors the current distribution between the resistors and its temperature dependence may have a remarkable influence on the overall TC value of the effective resistance (Reff = Usense/Itotal). This is especially true for non-symmetrical PC board layouts.

The objective of this investigation was to find a layout structure for the sense connection that is more or less insensitive to the layout of the current path, i. e. to the current distribution between the single resistors.

The following graphs show the PC board layout for both the current and sense structures as well as the results concerning the final resistance value (measured by Reff = Usense/Itotal) and the TC.
The test structures were manufactured using standard FR4 material with a copper thickness of 40 µm.

Explanations:



Results:

For both 2 and 3 resistors in parallel there is an optimum sense structure which supplies absolutely correct results for both resistance value and TC independent of the current lead position (i. e. the lead distribution) between the resistors.

See layout 4, 6 and 7 for 2 resistors
and layout 8, 9 and 10 for 3 resistors
in parallel.

The explanation for this result is that the sense structure is directly averaging the individual, slightly different sense voltages of the resistors.

On the other hand, a wrong layout may cause catastrophic results as shown in

layout 2 and 3
resp. layout 13 and 14

with TC values as high as +500 ppm/K or low as -770 ppm/K and variations of the total resistor value of +30 % to -25 %.

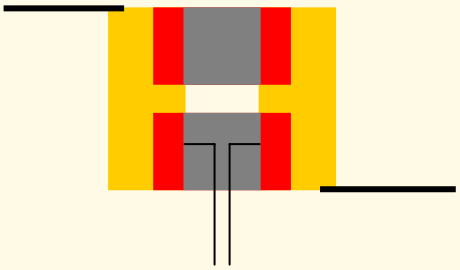
The actual R(T) curves for the resistors are shown on page 6. In the upper part the resolution is ±10 % showing the extremely bad results for the wrong layouts. In this plot the results of the correct layouts cannot be resolved from the horizontal axis (zero line).

The lower part of the graph shows the same results in a higher resolution (±1 %).
The maximum change of the resistors mounted on correct layout structures is the same for 2 or 3 resistors in parallel and even at the limits of the temperature range less than 0.1 %.

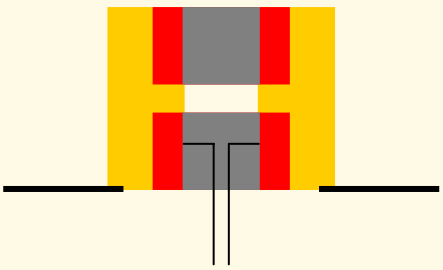
The graphs on page 5 show the actual PC board layouts used in an enlarged size of 5:1.

Part 1: 2 resistors in parallel (BVS-A-R001-1.0)

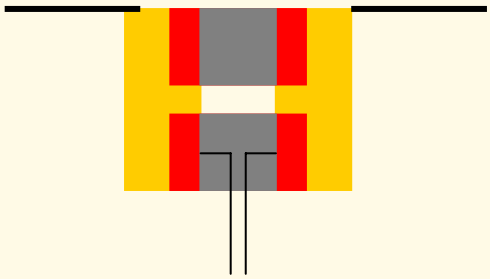
Geometry and experimental configuration with results for different layouts:



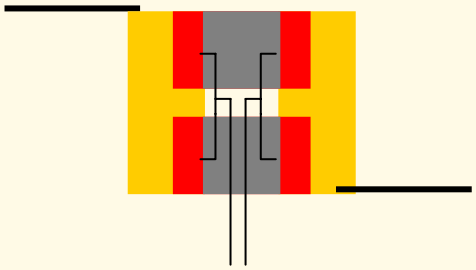
Layout 1:
TC: -5 ppm/K
R (20 °C) = 0.50 mΩ



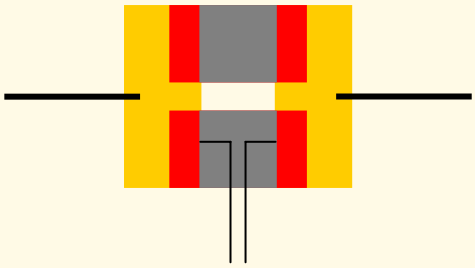
Layout 2:
TC: +370 ppm/K
R (20 °C) = 0.59 mΩ



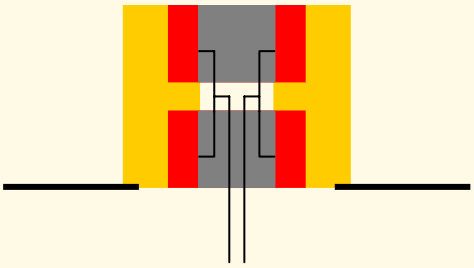
Layout 3:
TC: -560 ppm/K
R (20 °C) = 0.41 mΩ



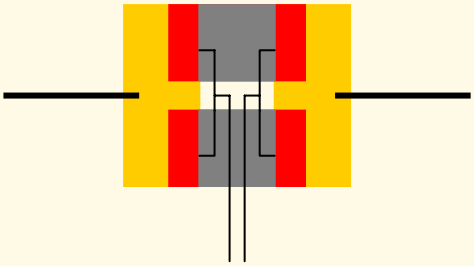
Layout 4:
TC: -3 ppm/K
R (20 °C) = 0.50 mΩ



Layout 5:
TC: 0 ppm/K
R (20 °C) = 0.50 mΩ



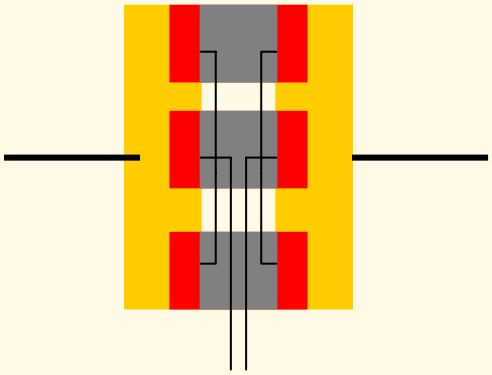
Layout 6:
TC: 0 ppm/K
R (20 °C) = 0.50 mΩ



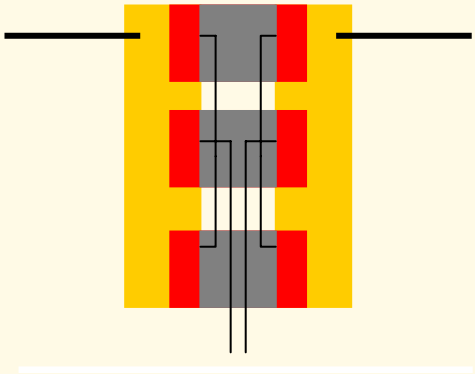
Layout 7:
TC: -2 ppm/K
R (20 °C)=0.50 mΩ

Part 2: 3 resistors in parallel (BVS-A-R001-1.0)

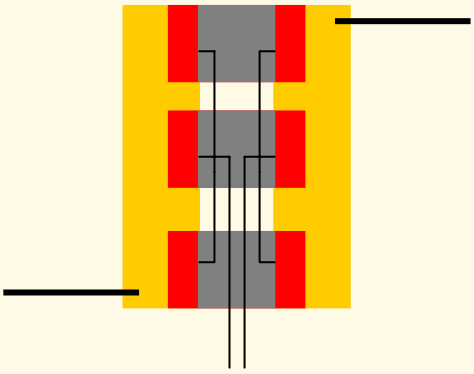
Geometry and experimental configuration with results for different layouts:



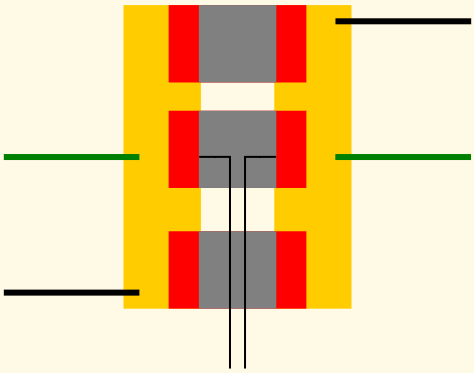
Layout 8:
TC: 0 ppm/K
R (20 °C) = 0.33 mΩ



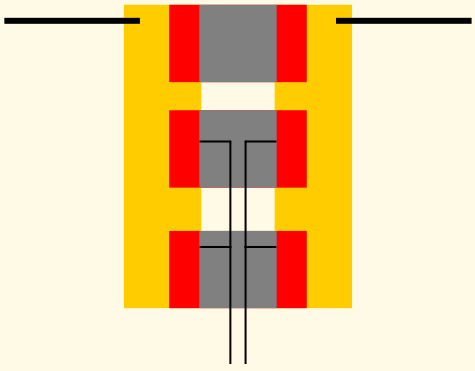
Layout 9:
TC: +3 ppm/K
R (20 °C) = 0.33 mΩ



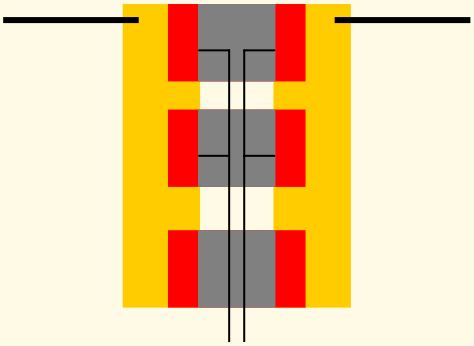
Layout 10:
TC: -3 ppm/K
R (20 °C) = 0.33 mΩ



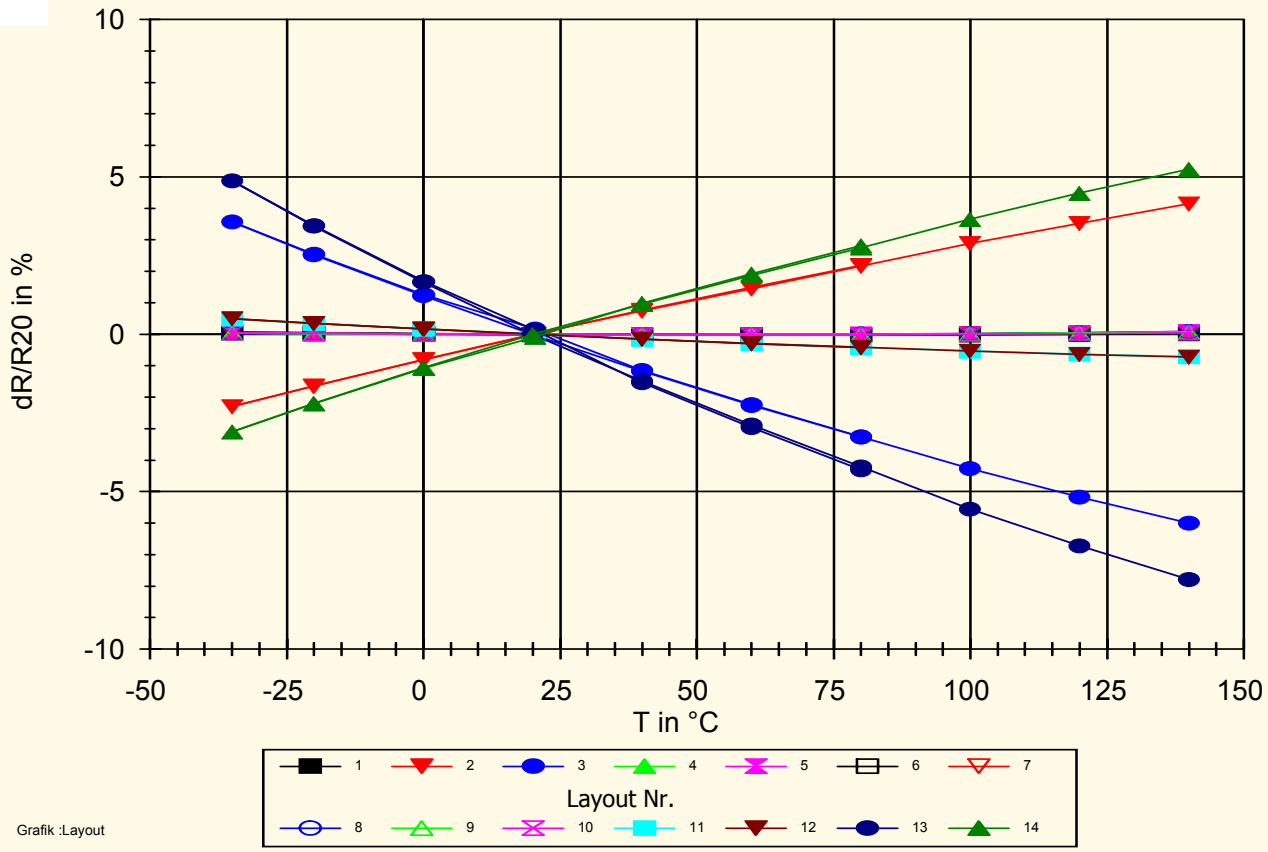
Layout 11 und 12:
TC: -75 ppm / K
R (20 °C) = 0.32 mΩ



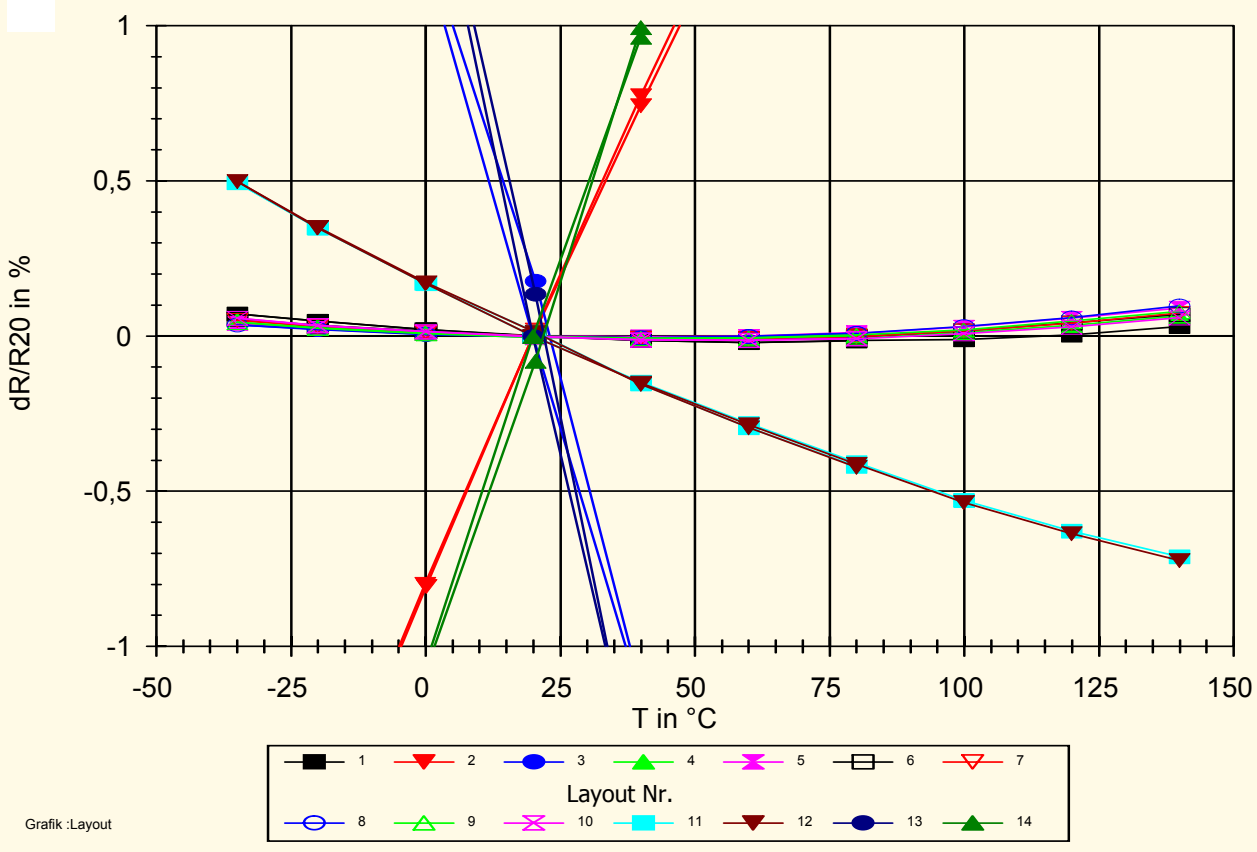
Layout 13 :
TC: -770 ppm/K
R (20 °C) = 0.25



Layout 14:
TC: +500 ppm/K
R (20 °C) = 0.43 mΩ

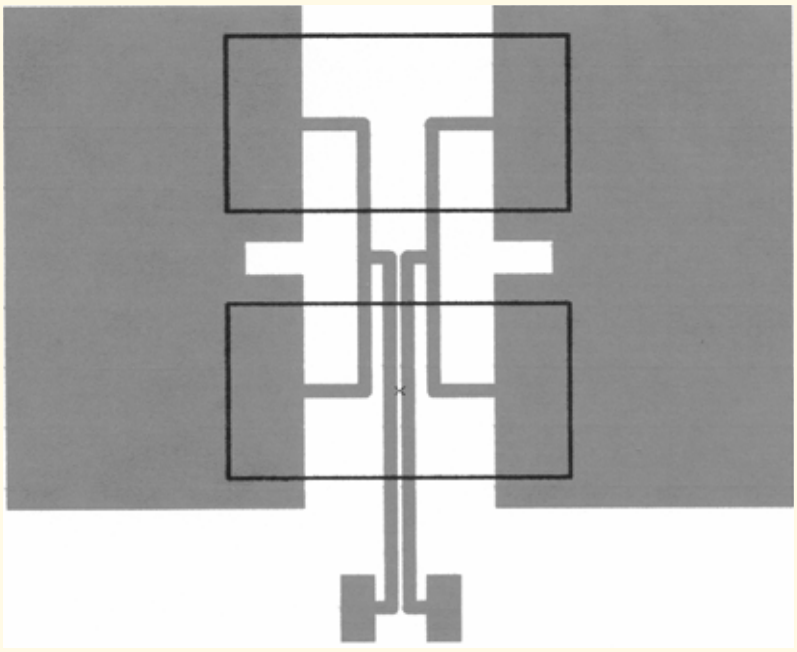


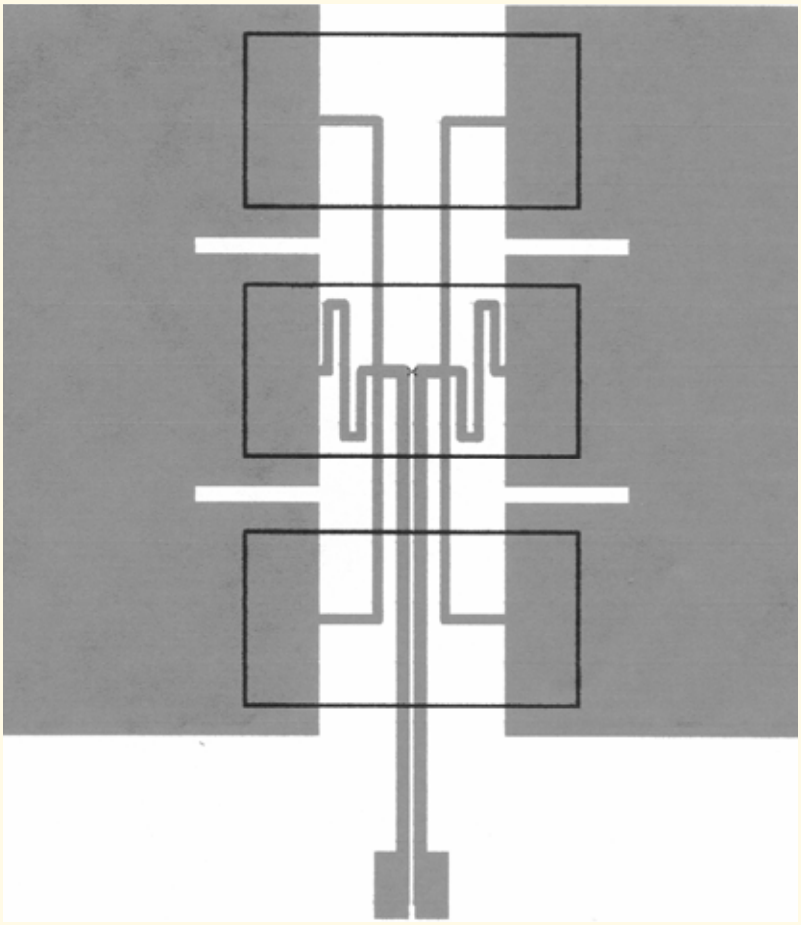
Grafik :Layout



Grafik :Layout

ISABELLENHÜTTE Application Report





Member of German Calibration Service

DKD

Cooperation with German Commission for Electrical, Electronic & Information Technologies of DIN and VDE

DKE VDE DIN

ISABELLENHÜTTE

ISABELLENHÜTTE Heusler GmbH & Co. KG
Eibacher Weg 3 - 5 · 35683 Dillenburg
P. O. Box 14 53 · D-35664 Dillenburg
Phone +49 27 71/9 34-2 50 · Fax +49 27 71/2 30 30
www.isabellenhuette.de · thermo@isabellenhuette.de

Member of AMA

AMA Fachverband für Sensorik e.V.

ISO/TS 16949:2002 and DIN EN ISO 9001:2000 certified

Issue 08/2007